Impact of On-Chip Inductance on Power Supply Integrity

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Motivation

- Power supply noise increasing problem, even for low power designs
- di/dt noise adds significant to the overall power supply noise budget
- On-chip inductance is claimed to contribute significantly to total di/dt noise
- Implementing on-chip inductance in power supply noise consideration increases complexity of design flow
- Can on-chip inductance still be neglected for timing considerations?
Scenario for Power Supply Nets

Regular power grid:
• Grid in close proximity to package power bumps

SoC power grid:
• No power bump connections in the outer region due to package and I/O restrictions
Simulation Setup

- \( V_{\text{Supply}} = V_{DD} - V_{SS} \)
- Power grid is modeled by a distributed RLC \( \pi \)-model
- ARM 926 core as reference module
  - \( I_{\text{peak}} = 0.52 \text{A} \) (for transient simulations)
  - Logic area = 1\text{mm}^2
  - \( f_{\text{max}} = 254\text{MHz} \), \( f_{\text{slow}} = 130\text{MHz} \)
- Flipchip package
  - \( 0.5\text{nH} \leq L_{\text{bump}} \leq 1.0\text{nH} \)
- Worst case cycle determined for
  - Position
  - Time (1\text{st}, 2\text{nd}, or 3\text{rd} cycle after load/frequency changes)
On-Chip Inductance

- Inductance determined through current loop (magnetic flux)
  - $L_{\text{eff}1} \neq L_{\text{eff}2}$
- Omitting mutual inductances as Worst Case estimate for inductance of power supply rails.
  (Current loop is infinite wide)
- $\frac{d}{dt}$ noise generation due to frequency change

Results:

- Different current profiles do not significantly increase power noise

\[ L_{\text{eff}} = L_{11} + L_{22} - 2L_{21} \]
Simulation Results for Regular Grid

- Cycle average of $V_{\text{Supply}}$ determines path delay degradation
- Comparison of $\Delta V_{\text{Supply max}}$ and $\Delta V_{\text{Supply avg}}$ without ($L_0$) and with WC on-chip inductance ($L_{WC}$)
  - Strong deviation between cycle average and maximal value
  - On-Chip inductance has significant effect on $\Delta V_{\text{Supply max}}$
  - Negligible effect on $\Delta V_{\text{Supply avg}}$
  - Similar results for varying $L_{\text{Bump}}$
  - On-Chip inductance still no impact on timing of logic blocks in regular power grid
Wire Distribution for Estimation of Effective Inductance

- Initial SoC grid simulations showed up to 20mV increase in cycle average power noise, omitting mutual inductances, i.e. Worst Case on-Chip inductance ($L_{WC}$)
- Absolute inductance of bumps and wires comparable
  - $L_{bump} \approx 0.5 \text{nH}$
  - $L_{wire} \approx 0.6 \text{nH} (L'/\mu\text{m}^*l_{wire})$
  - $Q(L_{bump}) >> Q(L_{wire})$
- Better estimate required by taking mutual inductances into account
- Detailed analysis of return path geometries
Estimation of Effective Inductance

Assumptions:

- \( C_{iso}/\mu m < 150aF/\mu m < C_{nest}/\mu m \)
- \( C_{min}/\mu m \rightarrow \) longest wires (WC)
- Caps < 4.0fF omitted (WC)
- Fanout 1 \( \rightarrow \) no branching (WC)
- Current return path only at the end of the wire (WC)
- Even current distribution (BC-WC)
- Worst case orientation of all wires
- Breakdown on different layers and their orientation
- Only orthogonal layers can increase current return path
Effective Inductance in Numbers

- Grid dimensions
  - \( \text{pitch}_{\text{LB}} = 400\mu\text{m} \)
  - \( \text{pitch}_{\text{M22B}} = 50\mu\text{m} \)
- Effective inductance \( (L_{\text{eff}}) \) is weighted mean of WC estimated current return paths
  - Mutual inductance is very short ranged
    - Fast saturation of inductance for increasing return paths
  - Percentage of return path (1) determines the effective inductance
  - Effective inductance close to best case (BC)

<table>
<thead>
<tr>
<th>return path</th>
<th>( L_{\text{BC}} )</th>
<th>2</th>
<th>( \geq 3 )</th>
<th>( L_{\text{eff}} )</th>
<th>( L_{\text{WC}} )</th>
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<tr>
<td>LB</td>
<td>99.2%</td>
<td>0.7%</td>
<td>0.1%</td>
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<td>L [nH/mm]</td>
<td>0.4</td>
<td>1.2</td>
<td>1.4</td>
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<tr>
<td>M22B</td>
<td>82.6%</td>
<td>13.2%</td>
<td>4.2%</td>
<td>0.68</td>
<td>2.1</td>
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<tr>
<td>pdf</td>
<td>0.5</td>
<td>1.4</td>
<td>2.1</td>
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Impact of On-Chip Inductance in SoC grid

- Increase of up to 20mV in power noise due to WC on-chip inductance
- For realistic estimate of on-chip inductance, impact of $L_{on-Chip}$ decreases to less than ±5mV
- Even in SoC on-chip inductance can be neglected for timing considerations under realistic assumptions
Conclusion

- On-chip inductance has significant impact on maximum power supply drop
- On-chip inductance might have impact on reliability (overshoots) and on-chip signaling
- Similar results for varying bump inductance
- Negligible impact of on-chip inductance on cycle average of $V_{\text{Supply}}$
- On-chip inductance still can be neglected in timing considerations for logic blocks