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Spectral PLL Built-In Self-Test for Integrated RF-Transceivers

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Kleinheubacher Tagung 2008



Motivation



Concept for Spectral PLL BIST



Stimulus Generation



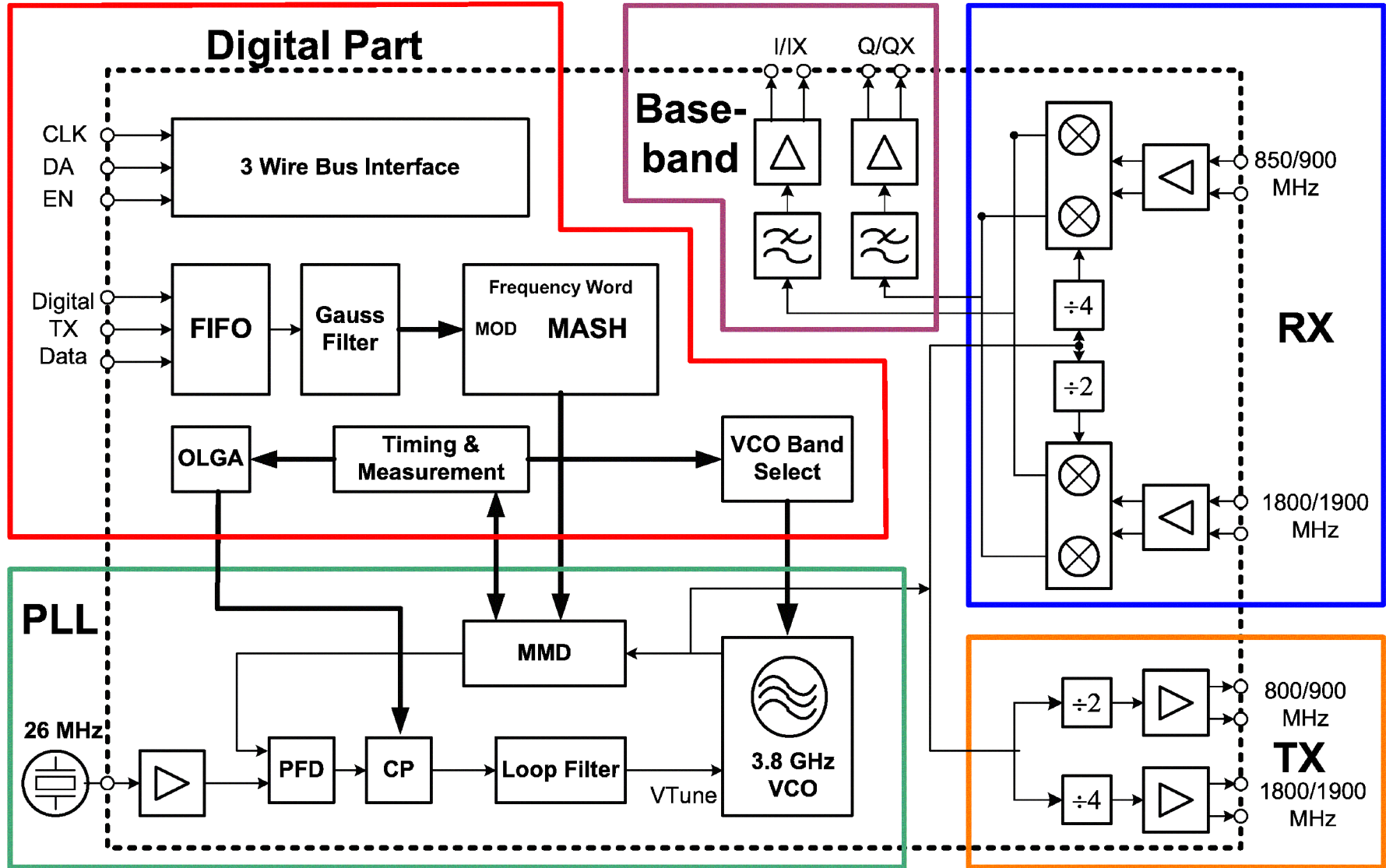
Spectral Response Analysis



Conclusion



Integrated GPRS Transceiver with $\Sigma\Delta$ – Modulator



Test Challenges for RF Systems-On-Chip

- System tests now have to be performed by foundry
- Many circuit blocks are no longer directly accessible
- Many RF tests are slow because of dynamic range
- Up to three test insertions for complex chips (D / A / RF)
- Increasing test costs @ falling production costs



Need to improve testability!



Critical Production Tests for RF PLLs

| Test | Challenge | BIST |
|--|--|---------------------|
| VCO / Divider Functionality | <ul style="list-style-type: none">- No direct access- Lots of failure modes | Time Domain ✓ |
| Loop Bandwidth | <ul style="list-style-type: none">- No direct access | Freq. Domain |
| In-Band Spectrum (Phase Noise, Spurs, Modulation Mask) | <ul style="list-style-type: none">- Complex signal analysis- High dynamic range | Freq. Domain |
| Out-of-Band Spectrum (Phase Noise, Spurs) | <ul style="list-style-type: none">- Long averaging times- Very high dynamic range | ??? |

RF PLL Test is complex and time-consuming!



Targets for PLL Built-In Self Test (BIST)

- Speed-up production test
- No interference with critical RF paths on-chip
- **Little area overhead**
- No yield losses due to test circuitry
- Direct correlation to specification (frequency domain!)
- Suitable for Deep Submicron CMOS technologies



Digital implementation of BIST circuits!



Efficient DSP Structures

- Robust filter topologies ► short wordlength
- Multi-rate signal processing ► low clock frequency
- Oversampling ► relaxed filtering requirements
- $\Sigma\Delta$ – signal processing ► single bit stream



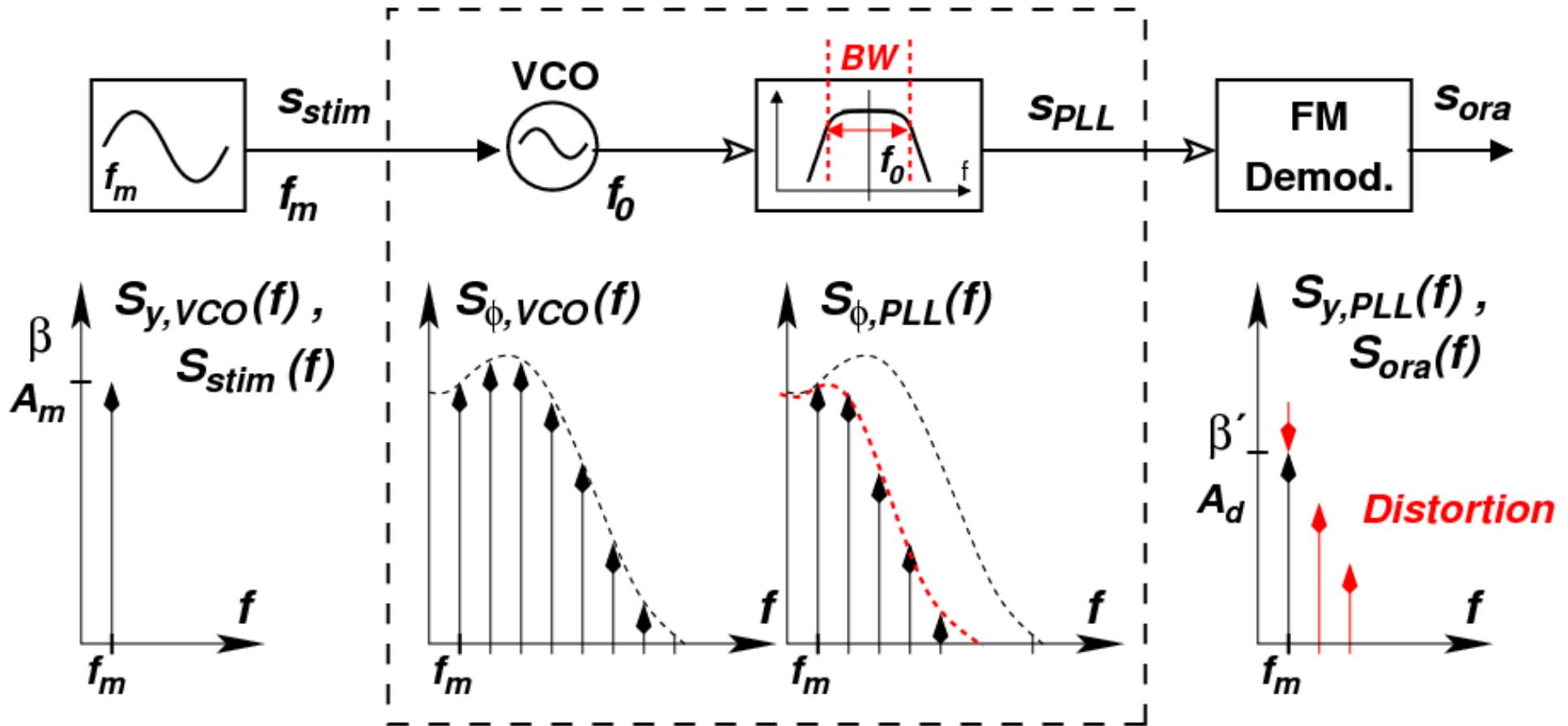
Outline

- Motivation
- **Concept for Spectral PLL BIST**
- Stimulus Generation
- Spectral Response Analysis
- Conclusion



Concept for Loop-Bandwidth Measurement

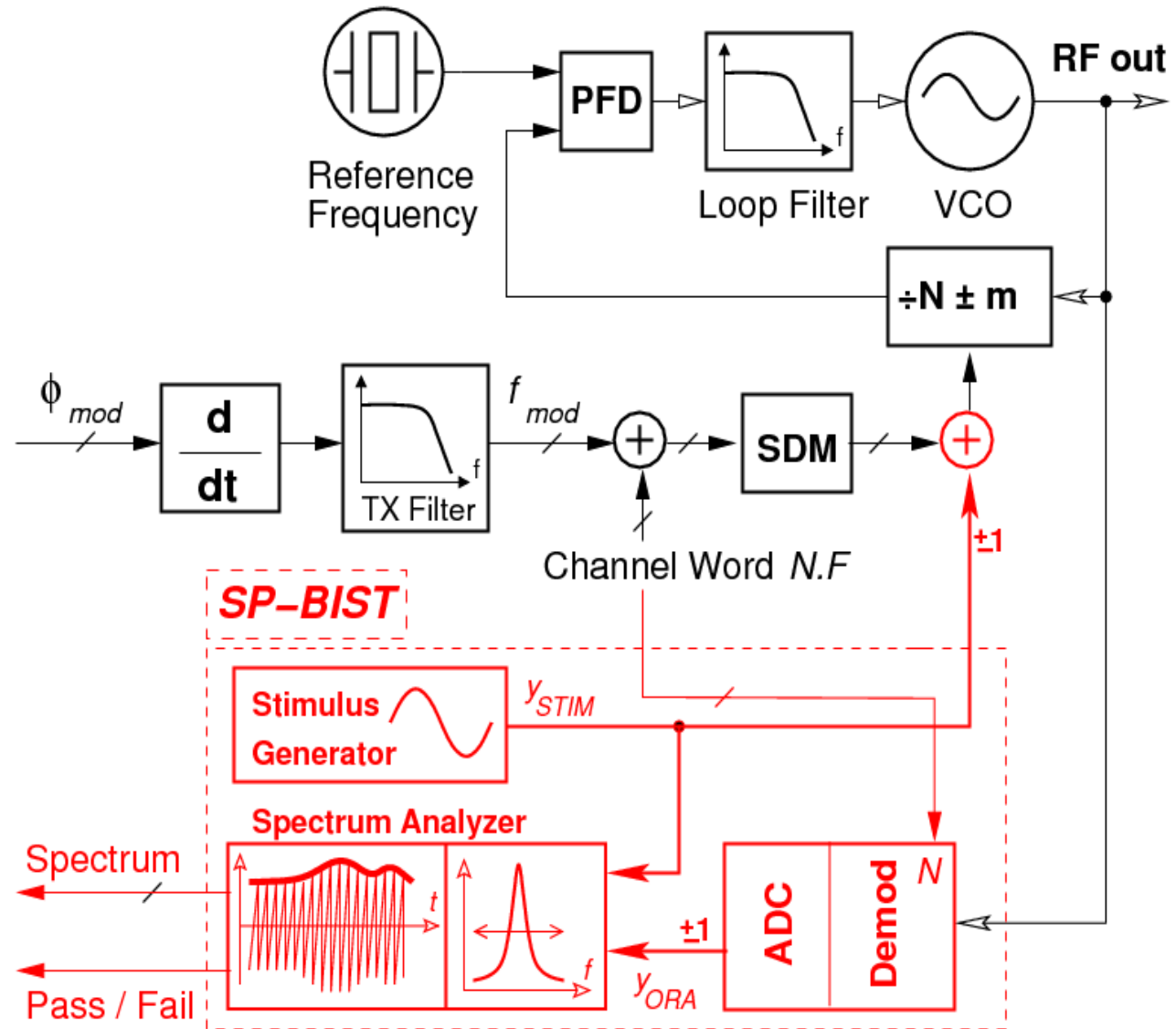
Circuit-Under-Test (CUT) : PLL



Estimate PLL bandwidth from FM distortion

Spectral PLL Built-In Self-Test (SP-BIST) - Details

- CUT is a $\Sigma\Delta$ -PLL with digital modulation input
- BIST is fully digital
- Minimum interaction with RF paths
- On-chip spectral analysis

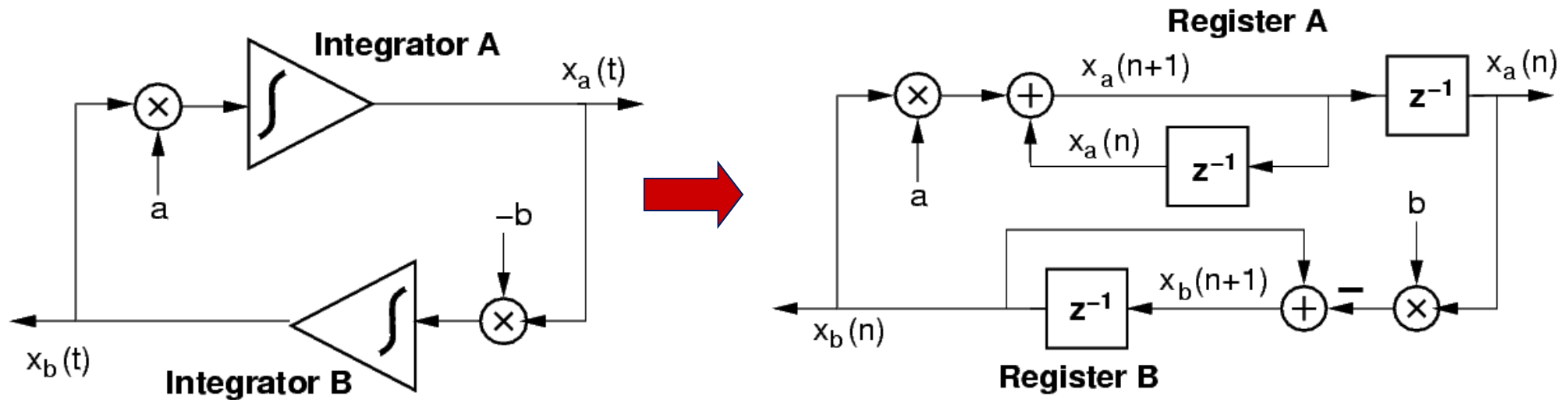


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Sine Oscillator Using Lossless Digital Integrators

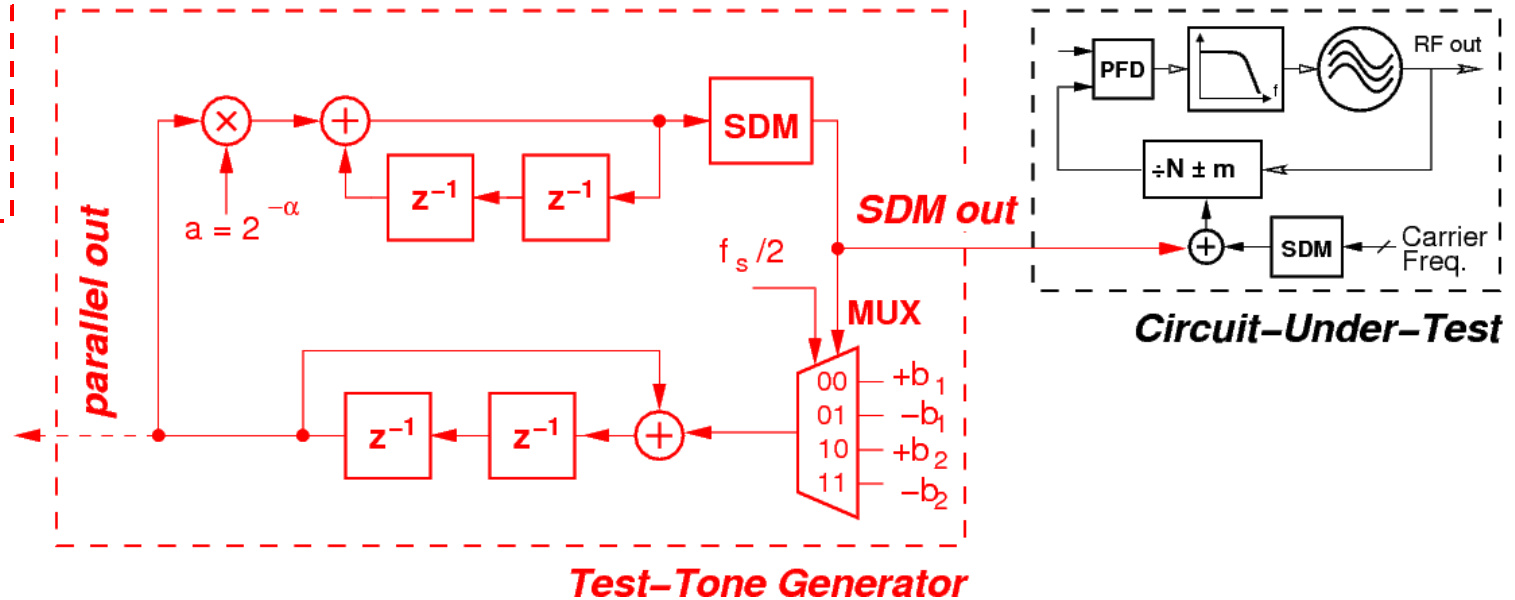


- 3 N-bit registers
- 2 N-bit accumulators
- 2 N x N multipliers

Test-Tone Generation

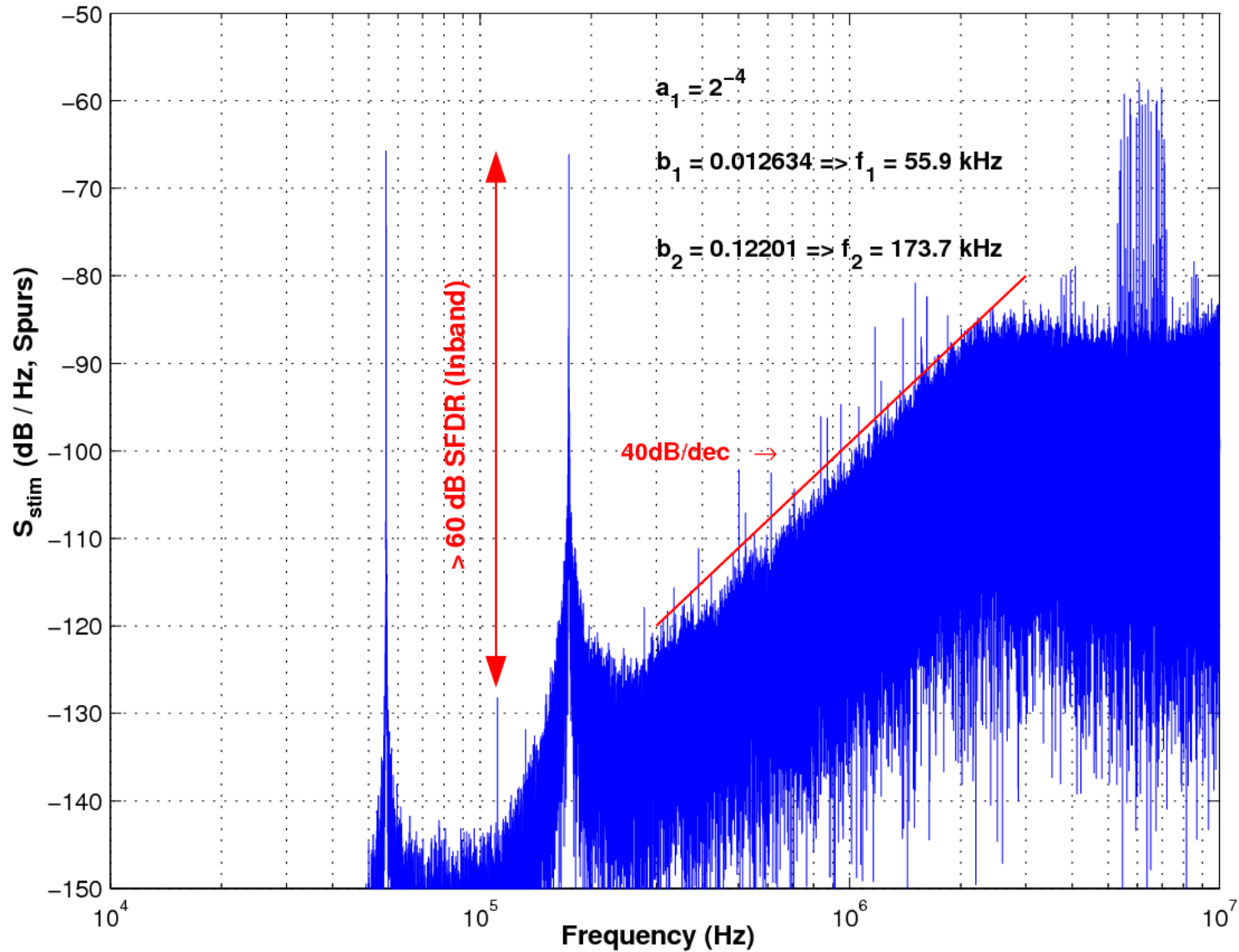
Lu & Roberts,
1998 CAS II,
[ADC BIST]

0.02 mm²



- Two-tone $\Sigma\Delta$ -modulated signal generated with digital resonators
- RF Modulation via digital PLL input
- No filtering needed due to inherent PLL low-pass characteristic
- $f_{\text{SIG}} = 15 \dots 180$ kHz with SFDR = 60 dB (15 bit wordlength)
- Also useful for DAC and analog filter test (with additional 1b-DAC)

Two-Tone Spectrum of Digital Sine Generator



Outline

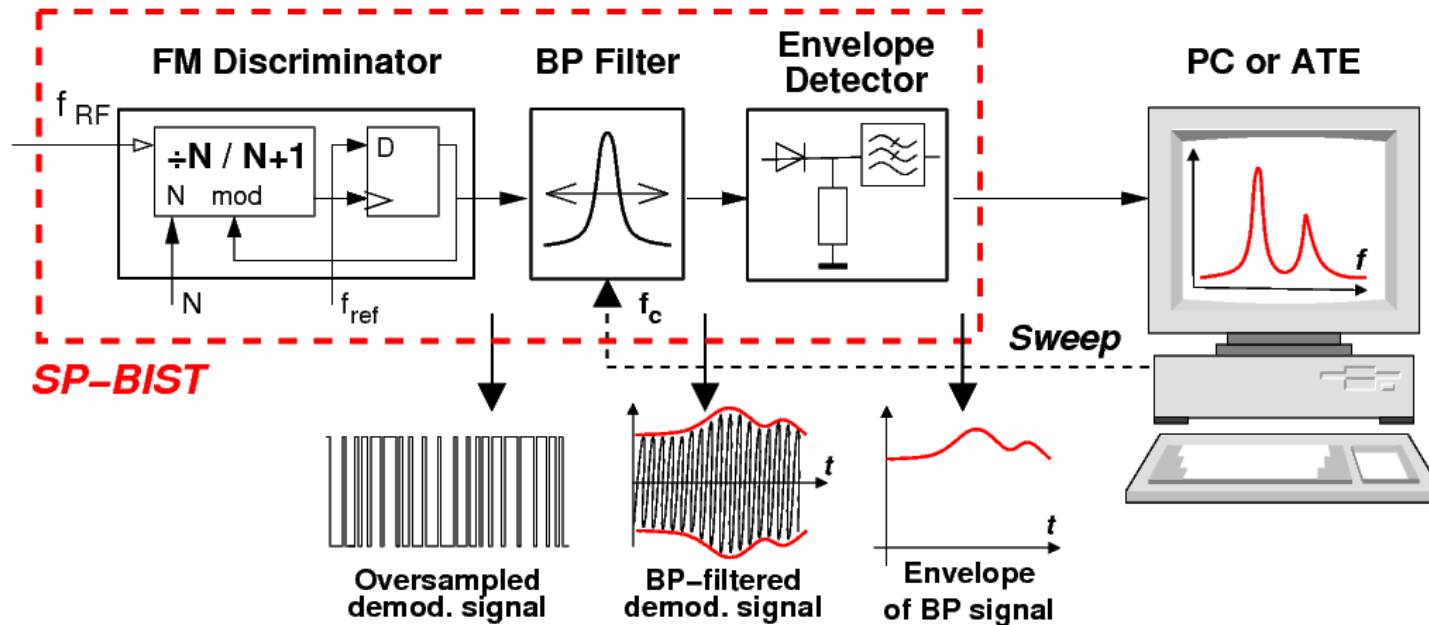
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Exploit Signal Properties for Spectral Analysis

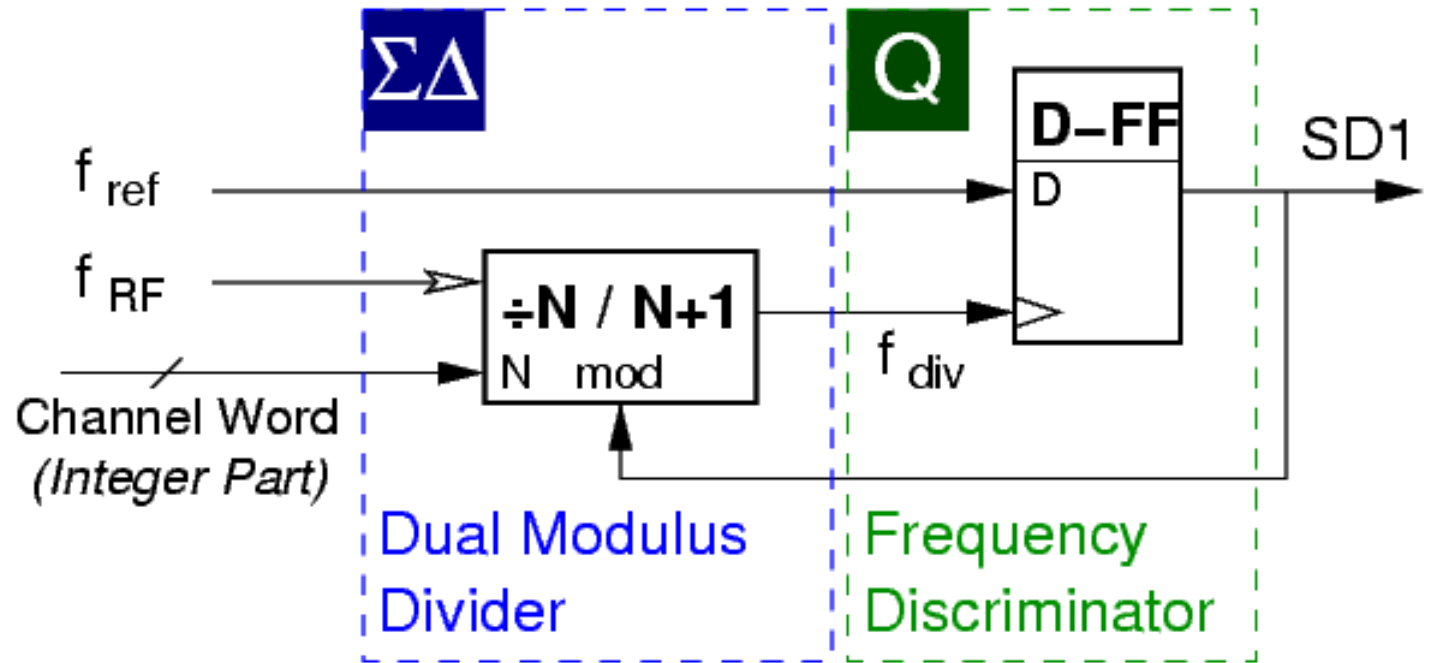
- Rail-to-rail signals on RF CMOS ICs
- Small bandwidth of PLL signal
- Carrier frequency is known on-chip
- Only FM / PM modulation

**Apply Digital
Signal Processing
Techniques!**



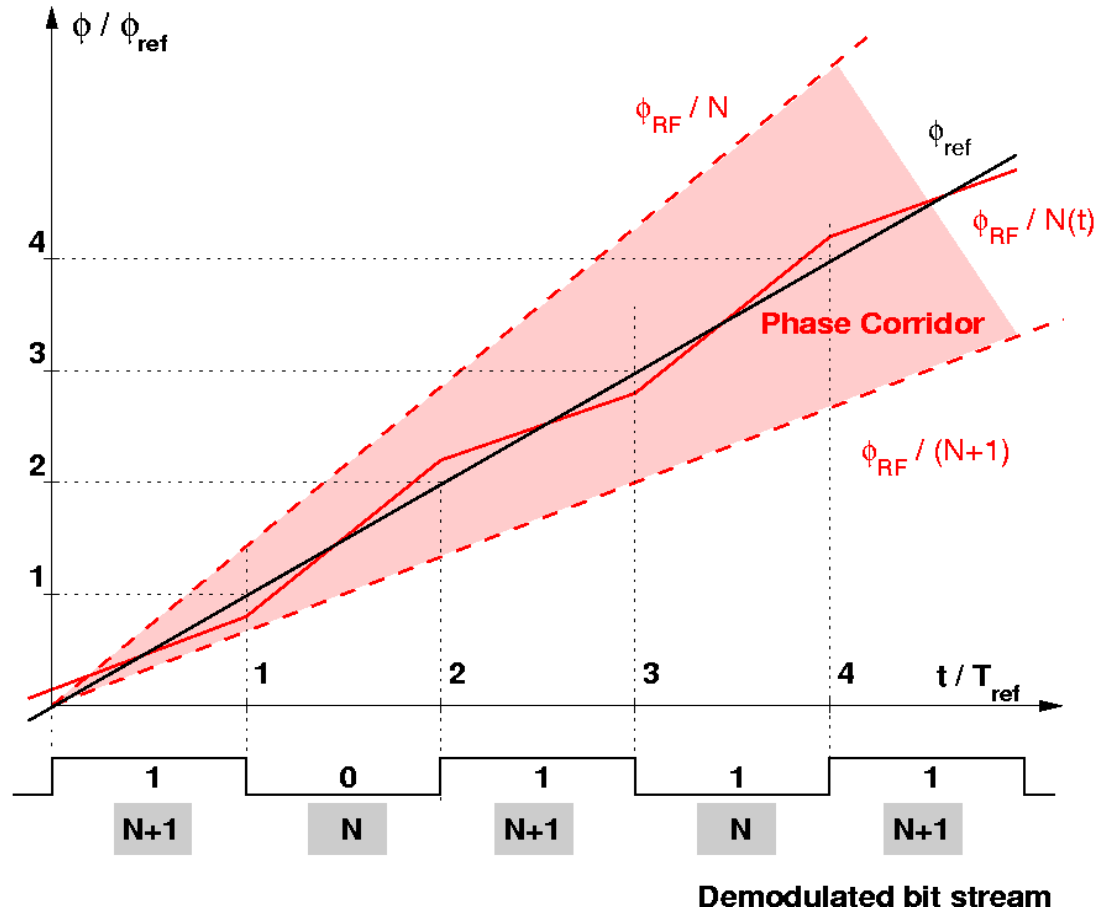
Sigma-Delta Frequency Discriminator (SDFD)

0.005 mm²



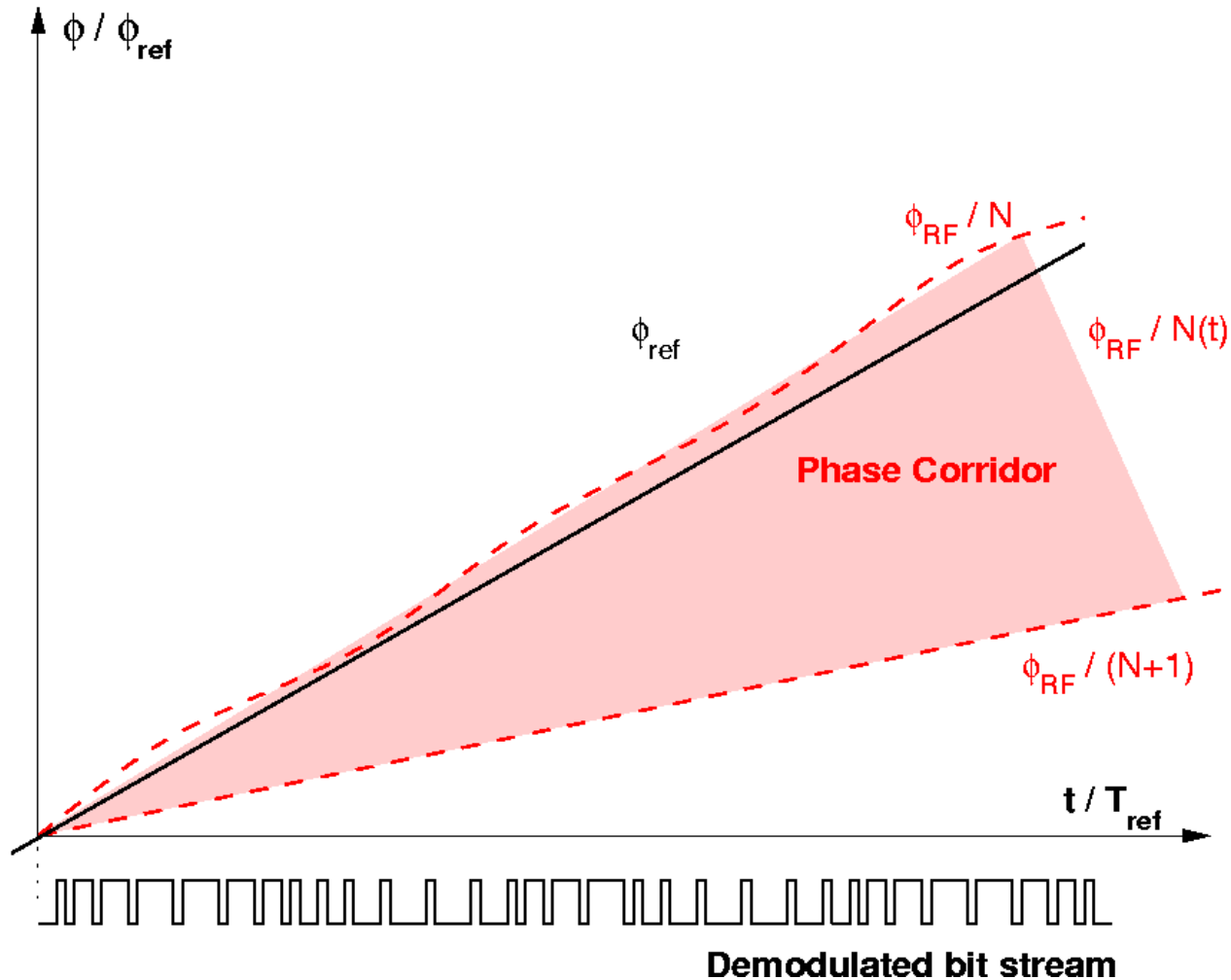
- RF (4 GHz) demodulation and quantization in one step
- Integrates / compares periods instead of amplitudes
- Building blocks can be copied from actual PLL
- Re-synchronisation to f_{ref} needed (not a big problem)
- **But:** *Lots of spurious sidebands (1st order SDM)!*

Principle of SDFD Conversion



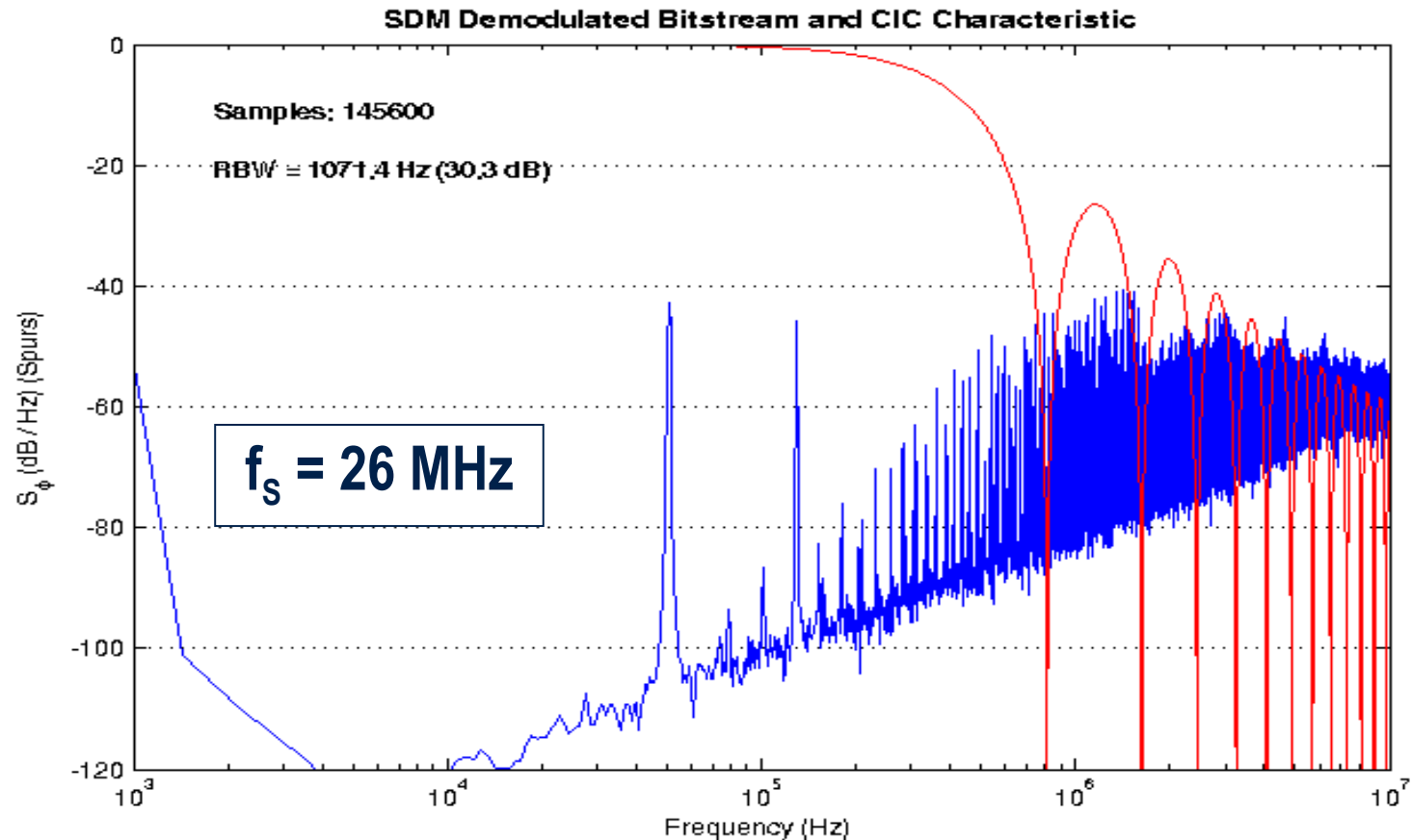
- Dual Modulus Divider operates as integrator + subtractor
- D-FF quantizes divided RF and reference phase

SDFD for Demodulation



Oversampled output bit stream contains modulation data

SDFD Demodulated Spectrum

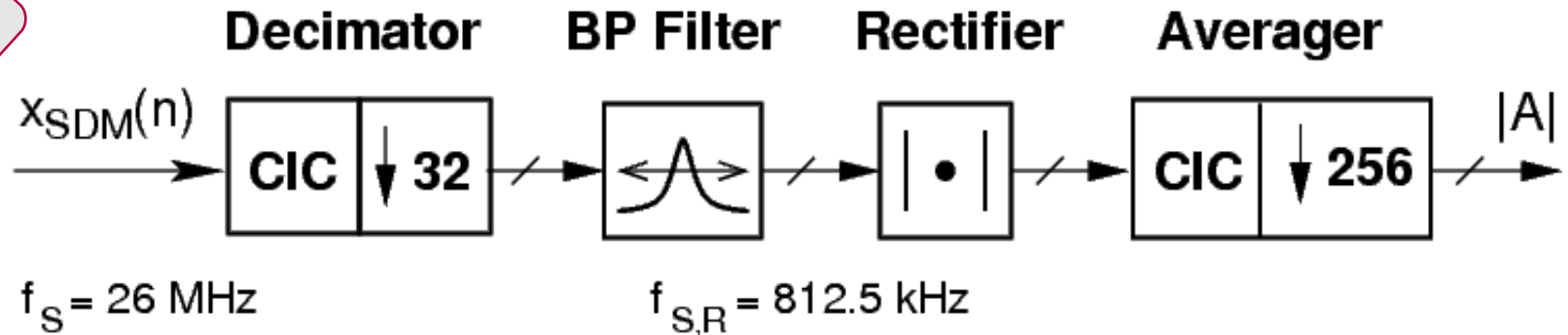


Quantization noise grows with 20db/dec. (1st order SDM)

Decimation filter needs to be at least 2nd order

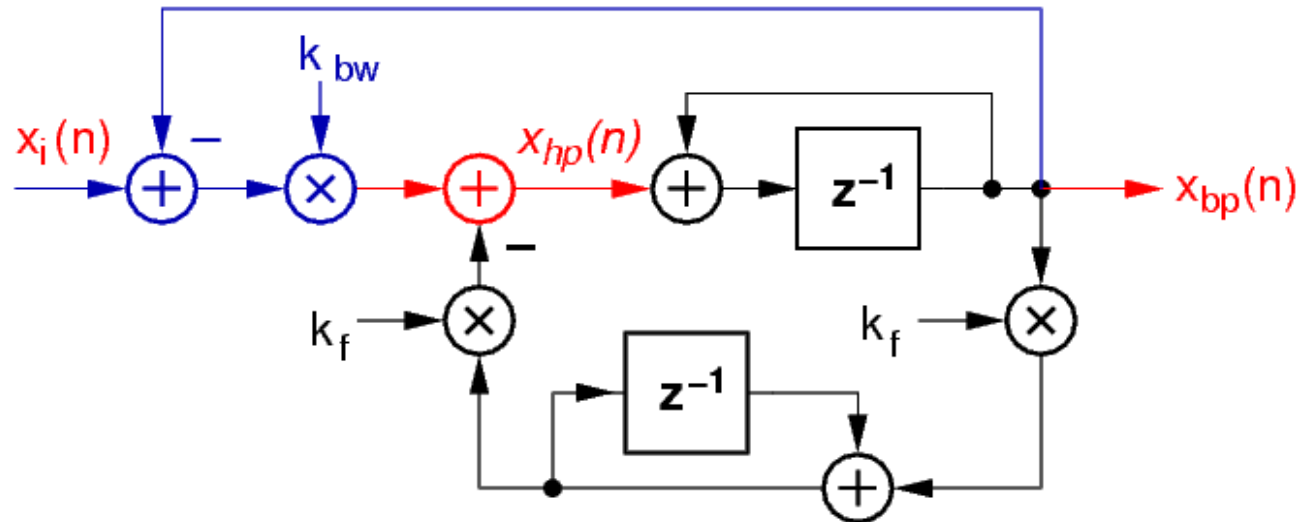
Narrowband Filter and Envelope Detector

0.035 mm²



- Spectral analysis by narrow-band filtering instead of FFT
- 4th order tunable BP with a freq. resolution of 300 Hz
- Multi-rate filter for lowest hardware requirements
- Bands of interest have to be measured sequentially
- Amplitude can be read via serial bus as static word

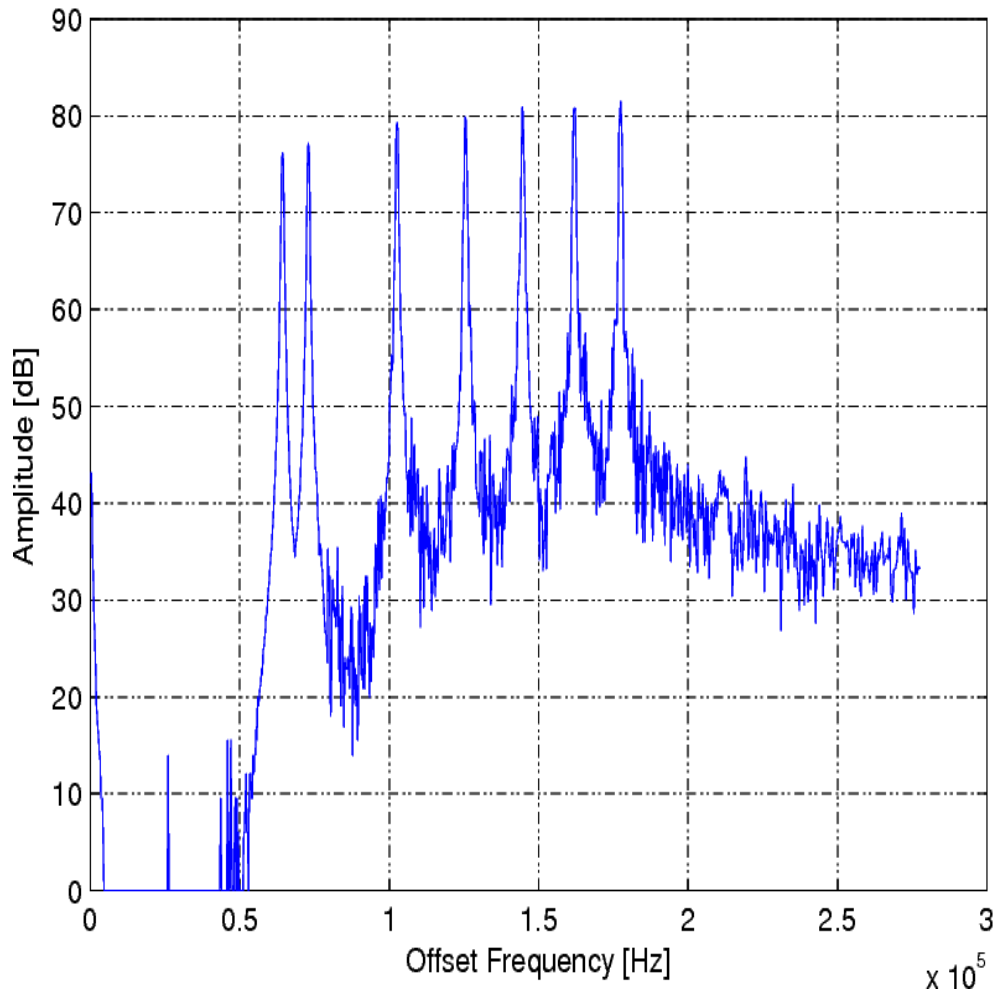
Digital Resonator as Tunable Bandpass



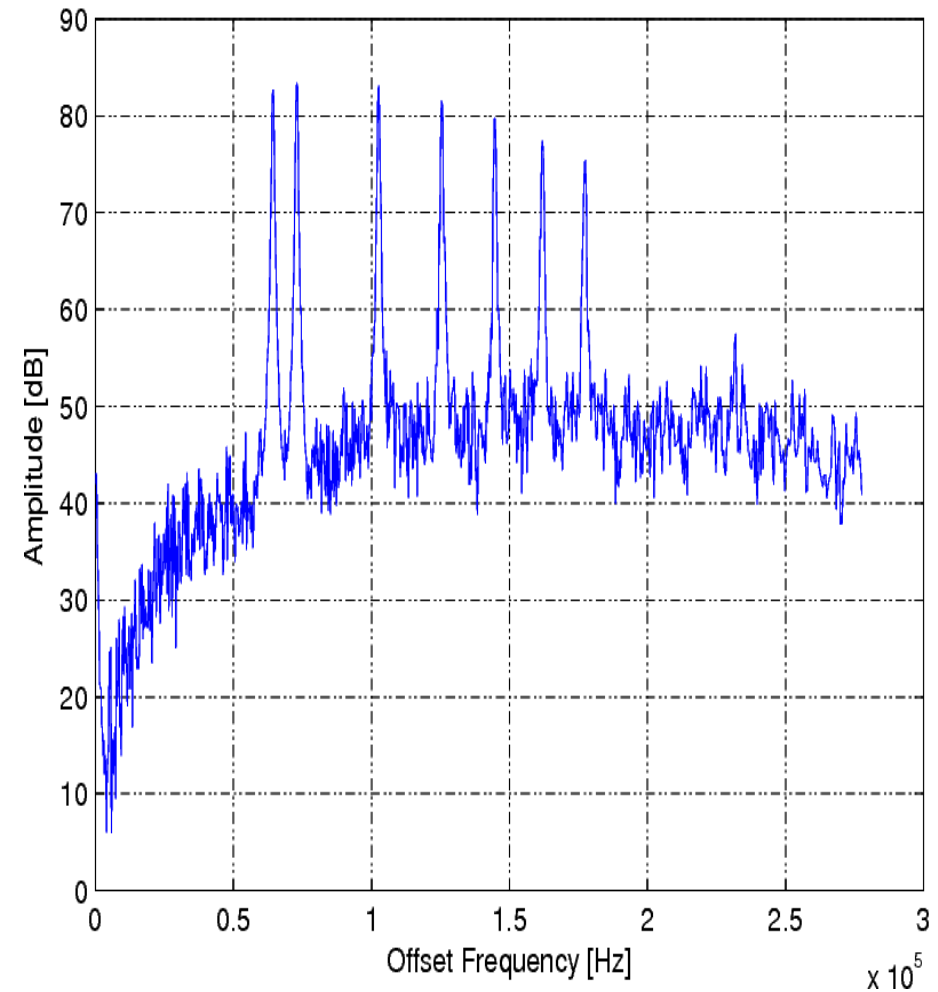
- Robust against coefficient truncation (only 9 bit wide!)
- Coeff. truncation error only influences center frequency
- Center frequency and BW can be set separately (k_f , k_{bw})
- Simple structure and low sampling rate enable hardware reuse
 - **Only 1 multiplier for 4th order bandpass!**
- Can be expanded to filter bank for parallel multi-tone analysis



Frequency Response Measurements (1)



Stimulus (Baseband)



Demod. PLL Response

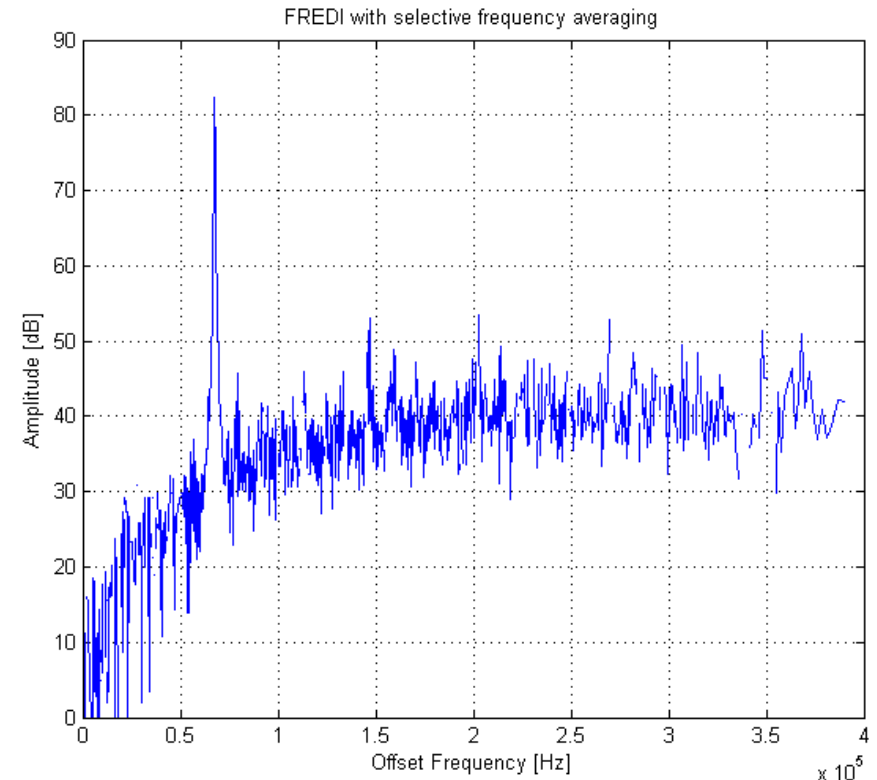
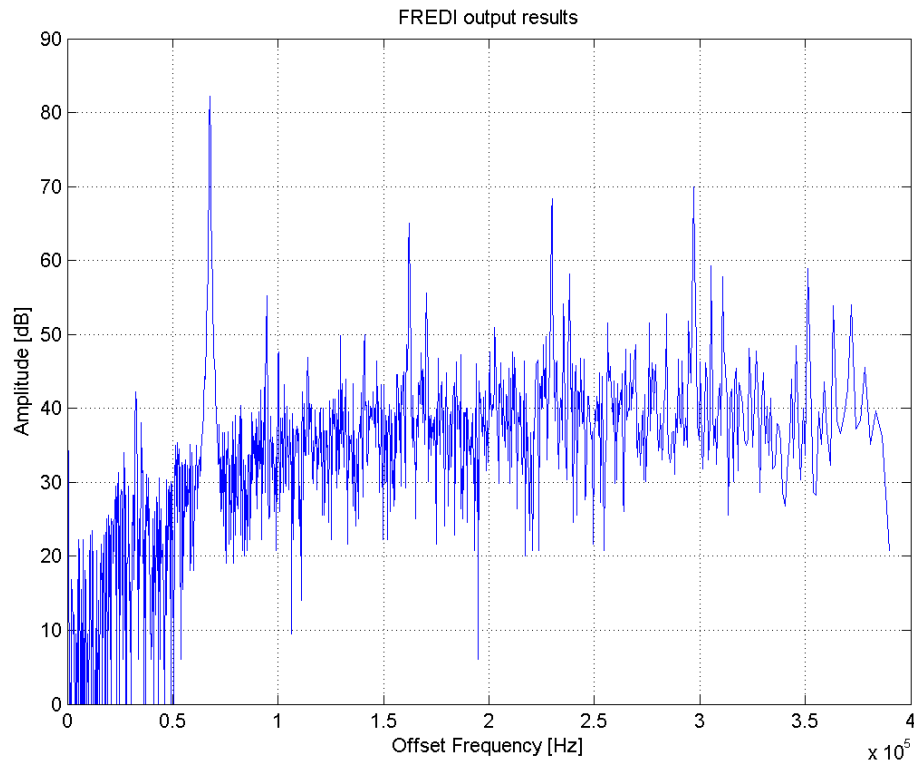
Frequency Response Measurements (2)

| | | | | | | | |
|-------------------------|----|-----|-----|-----|-----|-----|------|
| Frequency (kHz) | 64 | 73 | 103 | 125 | 145 | 162 | 177 |
| Attenuation (dB) | 0 | 0.3 | 2.7 | 4.7 | 7.5 | 9.7 | 12.5 |

- Performance of 1st order SDFD sufficient for loop BW measurement, but not for noise / spur analysis
- 3 ms measurement time per data point
- Wrong BP type (const. BW instead of const. Q) creates systematic error for discrete tones (can be compensated)
- Too narrow BP misses spectral maxima (+/- 0.3 dB)



„Frequency Averaging“ Removes SDFD Spurs



- Repeat measurements at different carrier freq. ($\Delta f = 10$ kHz)
- Remove data points differing by more than 10 dB
- “Frequency Averaging” improves spurs by ~ 30 dB
- Two-tone stimulus gives much better FSDM spur behavior

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Conclusion and Results

- Robust and compact Spectral BIST for RF PLLs (SP-BIST) has been realized in a 130 nm CMOS technology
- Two-tone test signals are generated with a completely digital test oscillator
- FM RF signals are demodulated and analyzed with a digital Sigma-Delta Frequency Discriminator and narrowband filter
- Spectral PLL BIST enables on-chip measurement of PLL bandwidth
- In-band noise and spurious sidebands can be measured with limited accuracy
- **Additional chip area for BIST blocks only 0.06 mm²**





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